REMARKS

This is in response to the Office Action dated December 18, 2008. Claims 1-20 were pending. Claim 1 has been amended in form only to replace the first instance of "comprising" with "having" and to replace the internal memory limitation of "for storing" with "configured to store." No other claims have been amended, canceled, or added. No new matter has been introduced. Upon entry of the amendments herewith, claims 1-20 remain pending. Reconsideration of the pending claims is respectfully requested in light of the discussion herein.

I. Objections to the Drawings

Page 3 of the final Office Action objects to the drawings for failing to show memory mapped input/output, a memory management unit, and a slave direct memory access (DMA) controller. It is respectfully submitted that these features are illustrated in at least the Interface 44 box of Figure 2. The particular features are described in the paragraph beginning at Page 3, line 6 of the present specification, and withdrawal of the objection is requested. The paragraph at Page 3, lines 6-10 is reproduced below for the Examiner's convenience (emphasis added),

> As mentioned above, the host controller 40 has a connection for the memory bus 32, which is connected to an interface 44, containing *a Memory Mapped Input/Output*, *a Memory Management Unit*, and *a Slave DMA Controller*. The interface 44 also has a connection 46 for control and interrupt signals, and registers 48 which support the RAM structure and the operational registers of the host controller 40.

II. Rejections under 35 U.S.C. § 103(a)

The final Office Action maintains rejections of all claims under 35 U.S.C. § 103(a) as allegedly unpatentable over ***Wang et al.***, **(U.S. Appl. 2002/0116565)**, hereinafter *Wang*, in view of ***Hamdi et al.***, **(U.S. Pat. 6,912,651)**, hereinafter *Hamdi*.

a. *Wang* does not teach a host controller adapted to act only as a slave

A broad analysis on Pages 4-5 of the final Office Action asserts that Fig. 1A of *Wang* discloses a host controller comprising a first interface for connection to a memory bus, which connects the host microprocessor and the system memory such that the host controller is adapted to act only as a slave memory on the bus. Paragraphs [0138-0140] of *Wang* are identified to explain *Wang's* Fig. 1A. The final Office Action further quotes text from a previous applicant response and asserts that *Wang's* requirement of "'involvement from the host microprocessor' makes clear that that host controller acts only as a slave device under the control of the microprocessor."

Applicants strongly disagree. *Wang* does not operate this way. *Wang's* host controller is not "adapted to act only as a slave on the memory bus." In fact, it is *Wang's* host controller that makes the decision of when bus access is necessary. So, while it is true that paragraph [0138] of *Wang* discloses a host controller 100 not having "bus mastering capabilities," it is clearly disclosed in paragraph [0139] that host controller 100 has an interrupt driven USB Engine 168 to send interrupts to the host microprocessor. That is, even though *Wang's* host controller is not a traditional "bus master," *Wang's* host controller is also not a slave. Instead, *Wang's* host controller is just a different type of master than a traditional "bus master." *Wang's* host controller still determines when bus access is desired, and his host controller sends interrupts to a host microprocessor in order to receive bus access. *i.e.*, *Wang's* host controller is performing the duties of a master in a way that is not like a traditional "bus master."

In contrast to *Wang*, the present invention claims a host controller "adapted to act only as a slave on the memory bus." In a preferred embodiment, host microprocessor 20 writes transfer based descriptors directly into the host controller 40 memory 50 or 56. See Page 4, lines 18-29. *i.e.*, In a preferred embodiment, the master host microprocessor 20 determines what action the slave host controller 40 will take. This is opposite of *Wang's* invention.

To summarize, the present invention has a particular master/slave relationship in order to copy transfer based descriptors. The microprocessor is a master. The host controller is a slave. The microprocessor directs; the host controller performs. *Wang* does not have the same

relationship as the present invention. Instead, in *Wang's* interrupt driven relationship, a host controller is a master, which makes requests via an interrupt, and a microprocessor is a slave that responds by executing an interrupt handler. Simply, *Wang* does not have a host controller "adapted to act only as a slave." Accordingly, claim 1 is allowable over the teachings of *Wang*. Reconsideration of the final Office Action analysis and rejections is respectfully requested.

b. *Wang* and *Hamdi* do not teach a direct connection to a memory bus

The final Office Action further admits that *Wang* does not disclose, teach, or suggest the "direct connection to a memory bus" of claim 1. Applicants agree. Page 5 of the final Office Action cites Fig. 6 of *Hamdi* to supply this missing feature of *Wang*, but *Hamdi* fails to cure the deficiency. Instead, the cited Fig. 6 of *Hamdi* is merely a recitation of the prior art admitted in the present specification at Page 1, lines 6-14. It is not disputed that *Hamdi* reduces access latency in the host controller by providing direct connection between system memory and the host controller, but the cited feature in *Hamdi* is nothing more than a conventional bus mastering host controller in a conventional electronic device. In fact, Fig. 6 of *Hamdi* is clearly described at Col. 11, lines 42-64 as a personal computer 600 wherein *Hamdi's* invention, a wireless USB transceiver, may be coupled to USB port 610 and connector 614 (both of which are outside of host controller 608).

In a previous applicant response, it was suggested that *Hamdi* did not expressly teach whether his host controller is a bus master or a slave. Obviously, however, *Hamdi's* personal computer 600 has a traditional bus mastering USB host controller. A personal computer would be expected to have nothing else. The previous applicant response did not persuade the Examiner with regard to involvement of the host processor, but the ultimate point of the discussion seems to have been missed. That is, if *Hamdi* were coupled with *Wang*, then the combination would fail to operate. *Wang's* interrupt driven system requires host controller 100 to interrupt host microprocessor 24 so that host microprocessor 24 can write data. *Hamdi's* bus mastering system requires host controller 608 to control the bus, which will stall microprocessor 602. If the *Wang* and *Hamdi* are combined, then either both the microprocessor and the host controller will try to control the bus and transfer data or neither the microprocessor nor the host

controller will control the bus and both will wait for the other to transfer data. Regardless, the combination will fail to operate. Accordingly, for at least the reason that *Wang* and *Hamdi* cannot be combined in any way that teaches the features of claim 1, withdrawal of the rejection is respectfully requested.

III. Conclusion

It is believed that the present independent claims are clearly patentable and that all dependent claims are also patentable. If the attorney of record (Thomas J. Satagaj) has overlooked a teaching in any of the cited references that is relevant to the patentability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact Mr. Satagaj at (206) 622-4900.

The Director is authorized to charge any additional fees due by way of this Amendment only, or credit any overpayment, to our Deposit Account No. 19-1090. Reconsideration of the present application in view of the foregoing amendments and the following remarks is respectfully requested. A Notice of Allowance is earnestly solicited.

Respectfully submitted,

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